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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,503	09/22/2004	PEI-HAW TSAO	TSMC 2003-1622	5502
44045 7590 06/14/2007 BAKER & MCKENZIE ON BEHALF OF TSMC 2300 TRAMMELL CROW CENTER 2001 ROSS AVENUE, SUITE 2300 DALLAS, TX 75201			EXAMINER FARAHANI, DANA	
			ART UNIT 2891	PAPER NUMBER
			MAIL DATE 06/14/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/711,503

Applicant(s)

TSAO ET AL.

Examiner

Dana Farahani

Art Unit

2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 May 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 16-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 16-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All   b) ☐ Some\*   c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC §102/ 103***

1. The following is a quotation of 35 U.S.C. 103(a) and 102(b), respectively, which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 16-18 and 20-26 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Koike et al. hereinafter Koike (US Patent Application Publication 2004/0036164).

Regarding claims 16, 17 and 26, Koike discloses in figure 10 a semiconductor package device, comprising:

a package substrate 2 having a first coefficient of thermal expansion and at least one bonding pad 6 on a surface of the package substrate; and

an integrated circuit chip 3 formed from a semiconductor wafer, the chip comprising: electrical devices formed therein (inherently in the chip),

at least one coupling structure 11 for bonding the chip to the at least one bonding pad on the package substrate; and

a final thickness less than a thickness of the semiconductor wafer (see paragraph 49), wherein the final thickness allows the chip to distort substantially with the package substrate during operational temperature changes despite the mismatch in their respective coefficients of thermal expansion (see also paragraph 65). A shape of the chip substantially conforms to a shape

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of the package substrate. As is stated in the reference, in paragraph 65, the final thickness of the chip is reduced to up to one forth of the initial thickness. A review of the reference reveals that smaller thickness reduction, i.e., larger final thicknesses relative to the initial thicknesses are also included in the reference. Therefore, noting that the present claimed invention reduces the final thickness of the chip to a ratio that is included in the reference, that is one third (see claim 17), it follows that the chip assembly of the reference is capable of performing the same function as that of the instant application, the function being the chip conforming to a shape of the package substrate during operational temperature changes.

Although, Koike does not expressly disclose a second coefficient of thermal expansion different than the first coefficient of thermal expansion, it is very likely that it is the case. Alternatively, assuming that the CET's are the same, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the substrate from different material (i.e. different thermal expansion) than that of the chip for the purpose of placing various electronic elements in the chip.

Regarding claim 18, Koike discloses the claimed invention, as discussed above, except for the numerical amount of the thickness of the chip. It would have been obvious to one of ordinary skill in the art at the time of the invention to make the chip with a desired thickness in accordance to how much pressure the chip would be handling during and after the fabrication of the chip. See *In re Boesch*, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980) for the proposition that discovering an optimum value of a result effective variable involves routine skill in the art.

Regarding claims 20-22, the coupling structure 11 is a lead free solder metal (Au); see paragraph 64.

Regarding claims 23 and 24, a dielectric encapsulant 12 is adjacent to a surface of the chip that is closest to the package substrate, and the one coupling structure is adjacent to the encapsulant.

Regarding claim 25, Koike discloses the claimed invention, as discussed above, except for the substrate is the material recited in the claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to select the material of the substrate from the materials recited in claim 25, in accordance to one of ordinary skill in the art preference of the material and cost considerations. See *In re Leshin*, 125 USPQ, for the proposition that it is within the general skill of a worker in the art to select a material on the basis of its suitability for an application. Note that substrate 2 has conductive traces therein (9 of figure 9).

3. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koike as applied to claim 16 above, and further in view of Huang (US Patent 6,559,525).

Koike discloses the claimed invention, as discussed above, except for a heat spreader coupled to the surface of the chip free of electrical devices.

Huang discloses in figure 7, heat sink 370 coupled to a surface of the chip 330. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention to attach a heat sink to a surface of the chip of the Koike reference in order to dissipate heat which would be generated during the chip functioning.

#### ***Response to Arguments***

4. Applicants' arguments filed 5/10/07 have been fully considered but they are not persuasive.

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I signed this, so if you  
can correct this page w/out Page 5  
affecting the pagination, you can go ahead  
& turn it in.

Applicants argue that the Koike reference does not disclose selecting the thickness of the chip so that the chip distorts in accordance with the package substrate during temperature changes.

This argument is not persuasive, because as discussed above, the thickness of the chip is in fact less than that of the substrate, and is reduced about the same amount as that of the claimed invention. Therefore, Koike inherently discloses the selection of the thickness of the chip, so it distorts in accordance with the package substrate during operational temperature changes. Moreover, if the chip wouldn't distort with the package, then it would break and become defective. Since the device in the reference patent presumably would not become defective during operation, the chip must conform to the substrate distortion during temperature changes.

Applicants' argument that the grinding in the Koike reference is expressly done to fit the package within a certain dimension, while in the claimed invention grinding is done to so that the chip distorts substantially with the substrate is not persuasive. This is because regardless of the reason behind the grinding, the aforementioned distortion effect is produced by the reference, hence satisfying the requirement of the claim.

Finally, assuming, arguendo that the aforesaid "selecting thickness" is not thought by the Koike reference; although it is the <sup>position</sup> ~~poison~~ of the Office that it discloses that limitation, selecting a thickness of the chip is a <sup>mental</sup> ~~process step~~, and in a claim <sup>directed towards a product, the</sup> ~~where a device is claimed~~, that process step ~~has little, or no patentable weight.~~ <sup>well-established product-by-process doctrine</sup> makes it clear that the burden is on the Applicant to provide evidence that a structural difference exists. <sup>The</sup> ~~Applicants'~~ arguments relating to applicants' ~~the~~ subjective motivation do not constitute factual evidence that any structural difference exists.

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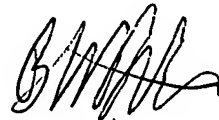
*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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**B. WILLIAM BAUMEISTER**

**SENIOR PATENT EXAMINER**

U.S. PATENT AND TRADEMARK OFFICE